



FIG. 1

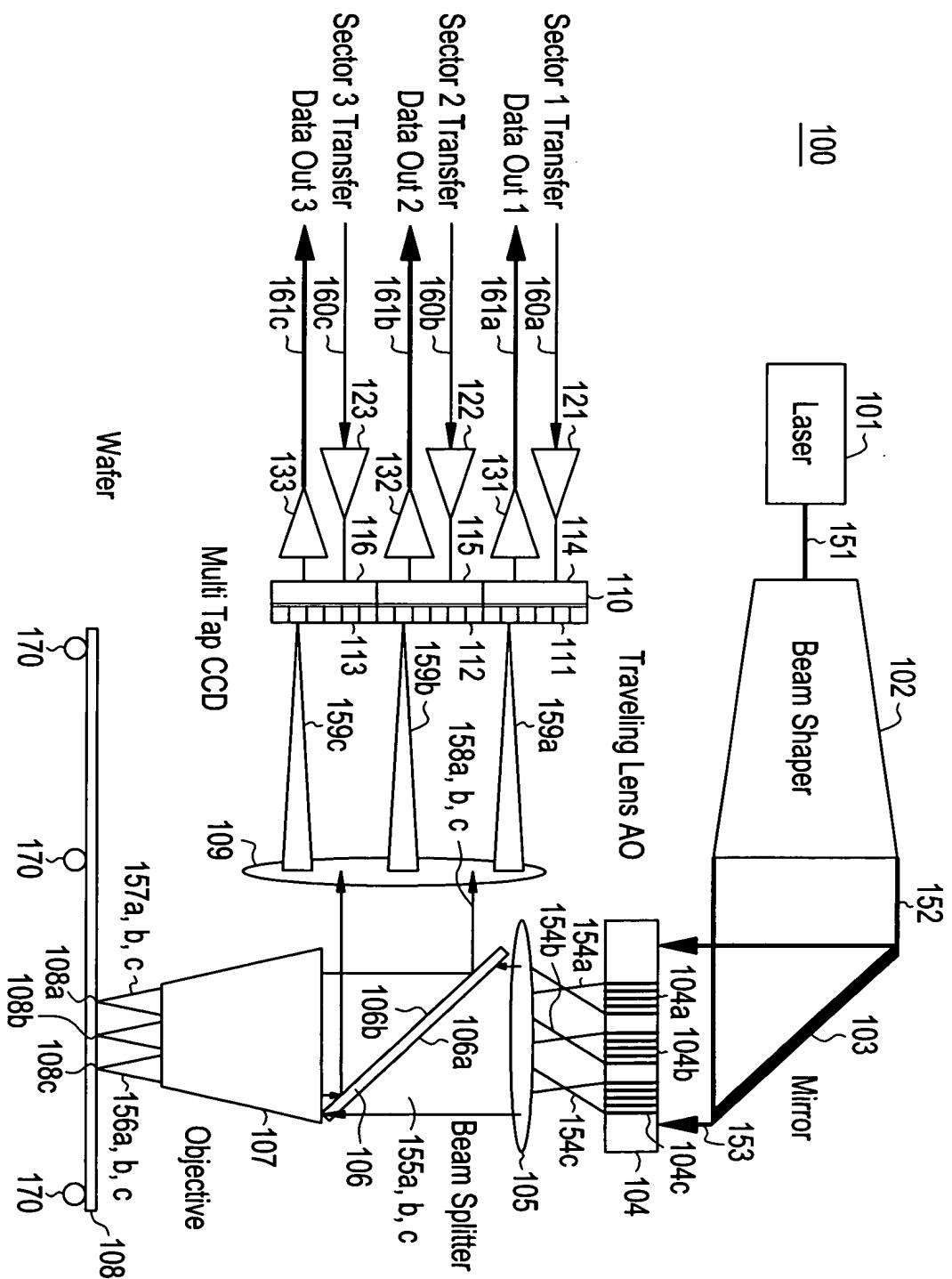


FIG. 2

CCD Timing Diagram

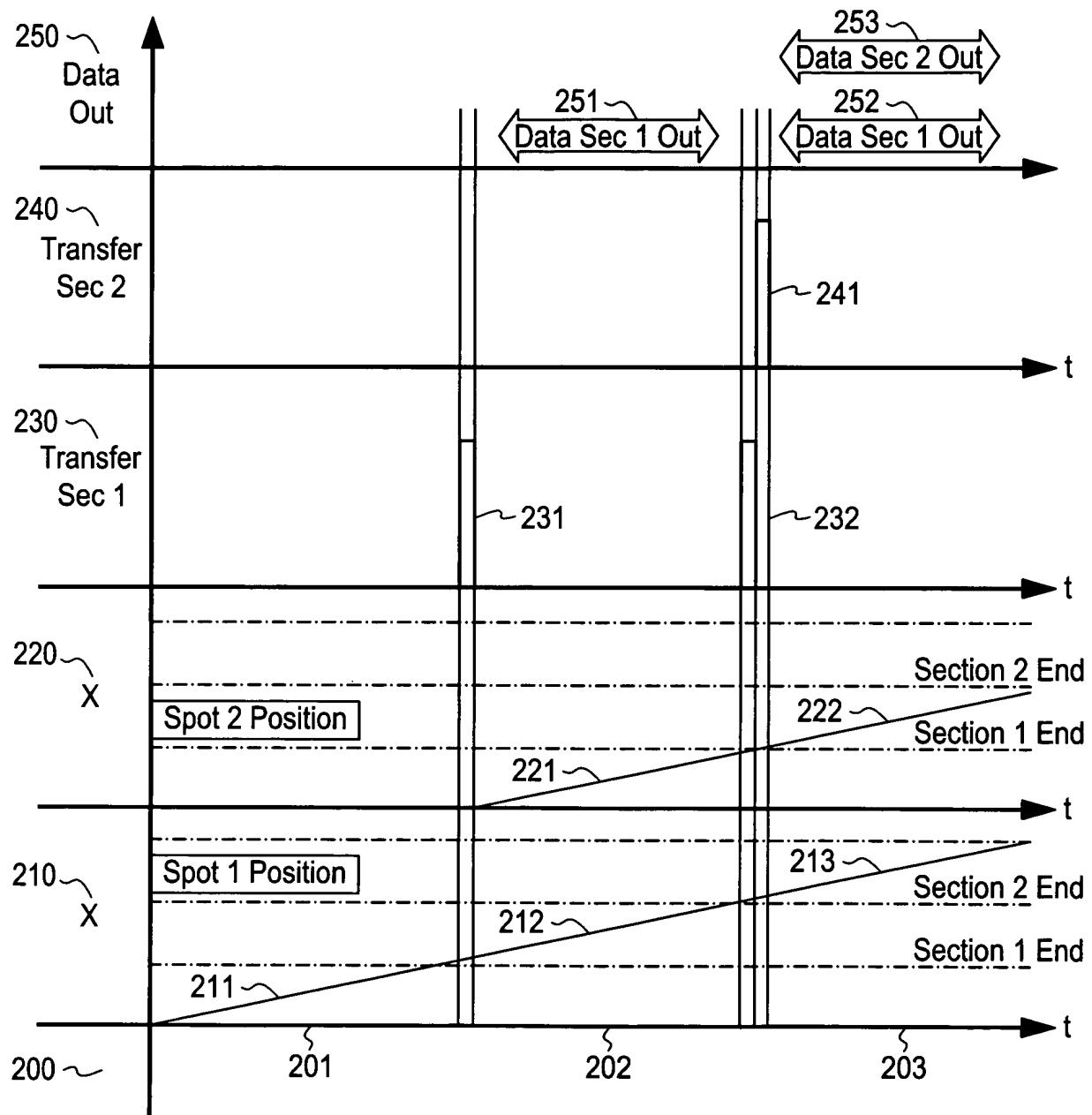


FIG. 3

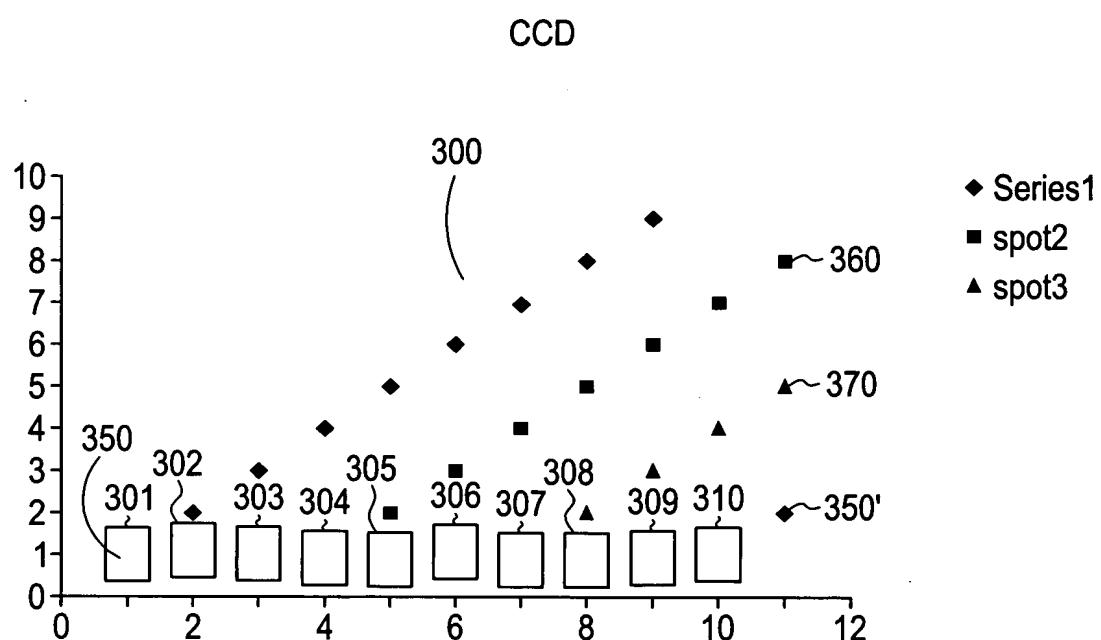


FIG. 4

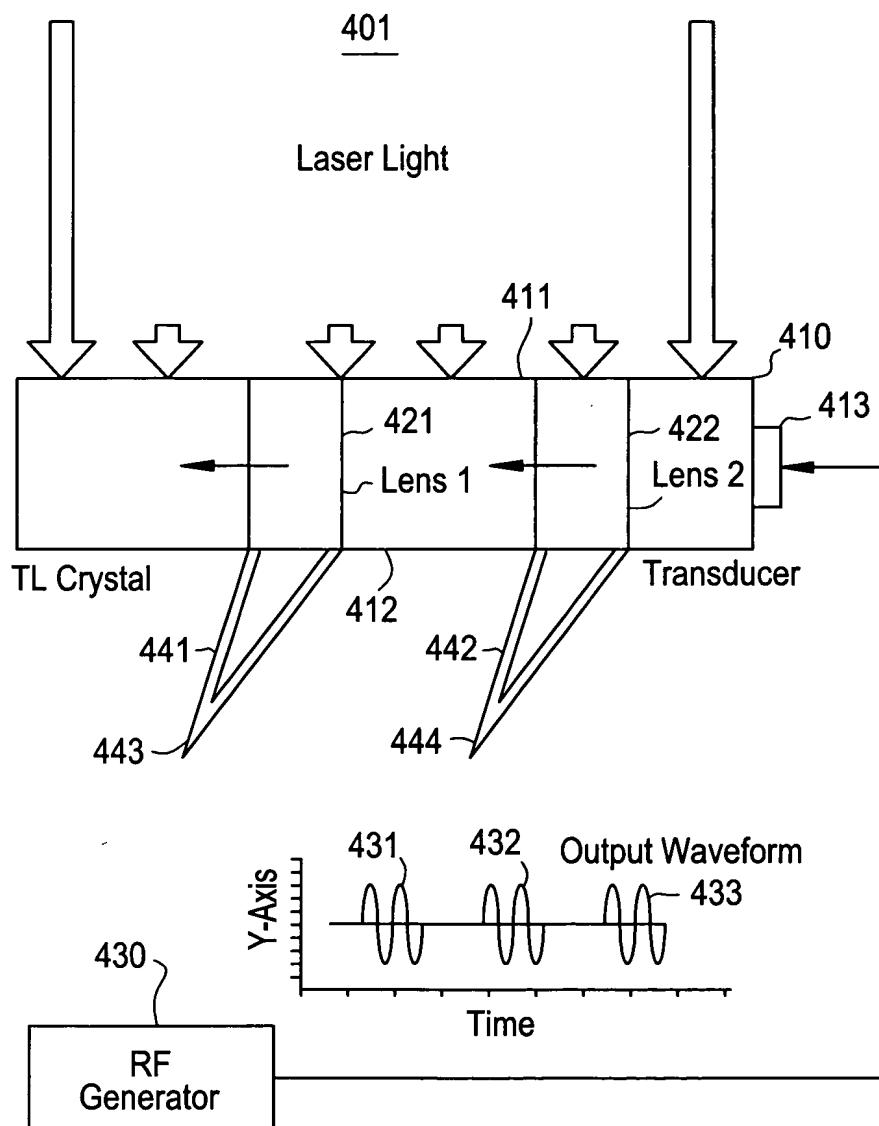


FIG. 5

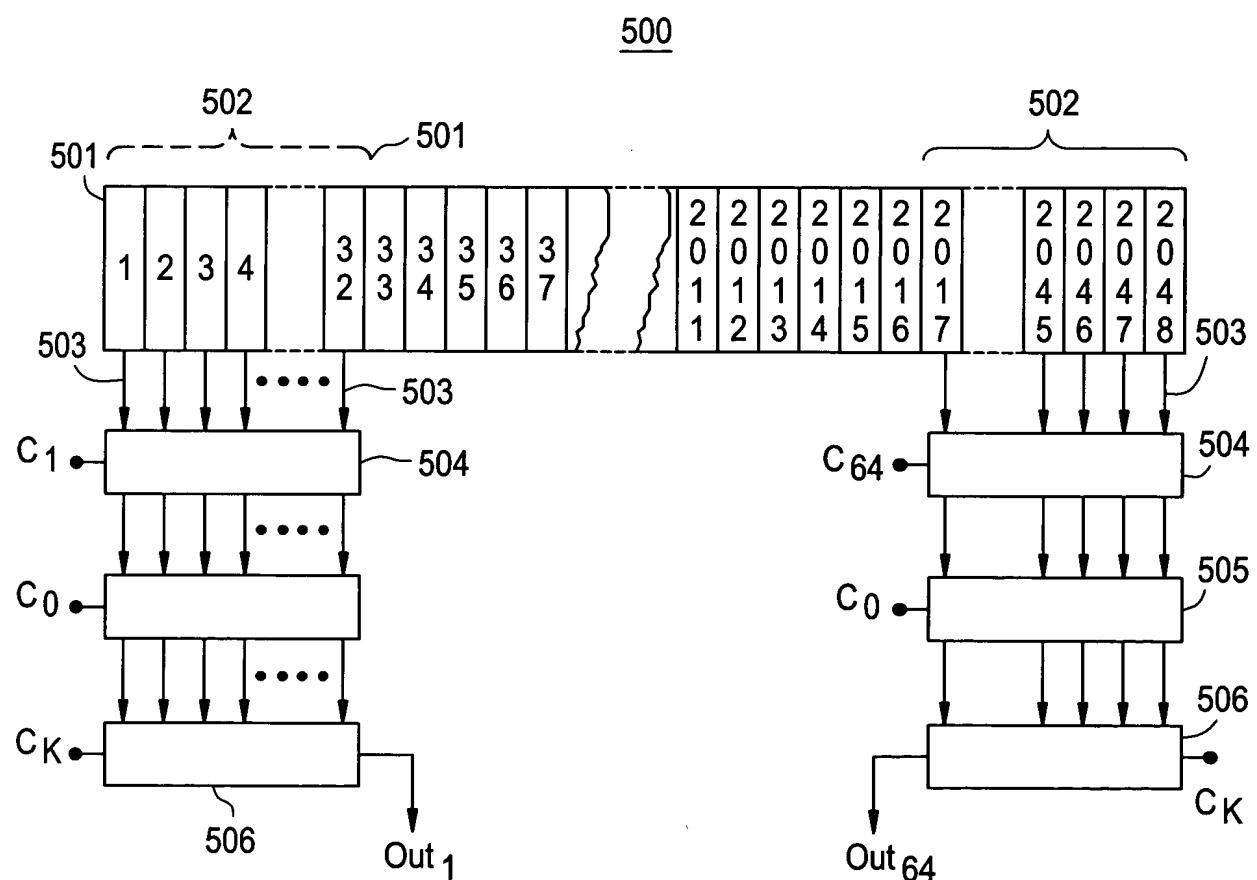


FIG. 6A

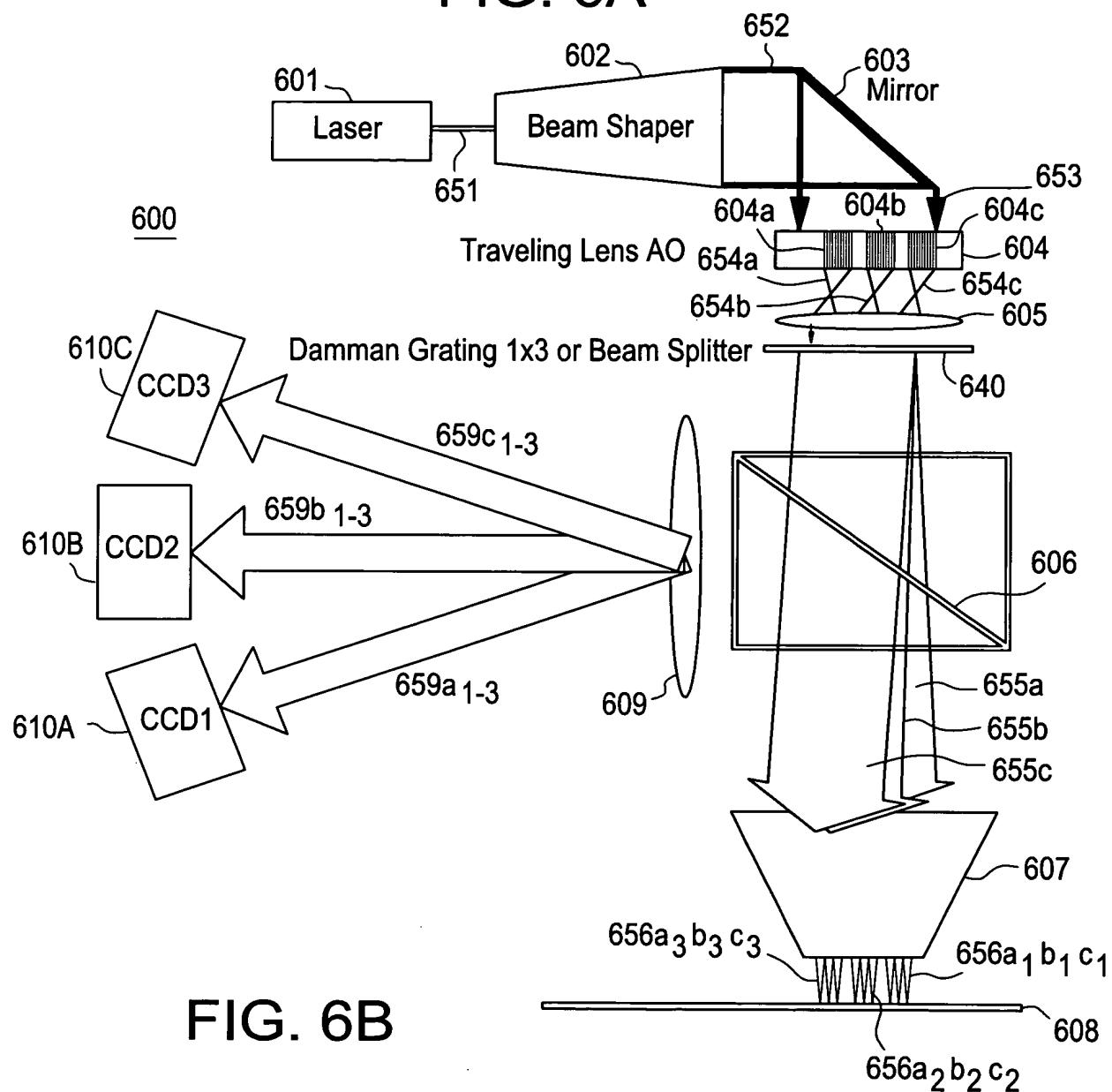
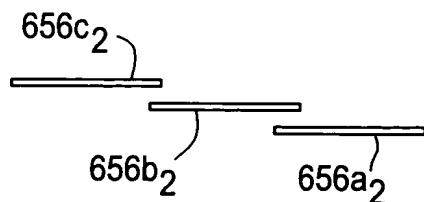


FIG. 6B

Line Structure on WAFER



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FIG. 7A

